REMARKS

Original claims 1-16 are canceled. Claims 17 and 27 are amended herein to include the limitations of claims 22-23 and 28-29 respectively, which are canceled. Claims 22 and 30 are canceled.

Claim Rejection Under 35 USC 102(b)

Claims 17-21, 27 and 30-31 are rejected as being anticipated by Ryan (US Pat. No. 5,675,654). Ryan discloses a transport decoder system designed for decoding a transport stream including transport PES packets, which is coupled to a NRSS Smart Card for decryption of at least part of the transport stream. The transport system comprises a decoder (110) connected to a physical layer channel interface (112), external buffer memory (114), a host microprocessor (116), external video and audio decoders (118 and 120) and a clock signal circuitry (122). Decoder 110 contains a transport processor 214 that parses the datastream packet to extract a PID and compares the PID with entries in a PID Table maintained in the transport processor. The PID table is set up under software control by the host microprocessor 116. If a match is found, the data in the packet is processed according to the matching PID Table entry, which assigns a DMA channel number. After separating the packets according to their PID's and storing data from the packets in an appropriate FIFO module, the transport processor 214, in conjunction with memory controller 216, stores data from the packets according to their PID's in sequential memory locations of the designated channel in the external memory 114.

As noted by the Examiner, Ryan does not clearly disclose the limitations of dependent claims 22, 23, 28 and 29. Independent claims 17 and 27 are amended to include these limitations and are therefore distinguishable over Ryan. Claims 18-21 are dependent on claim 17 and claims 30-31 are dependent on claim 27 and thus include the distinguishing limitations. For these reasons, withdrawal of the rejection is respectfully requested.

Claim Rejection Under 35 USC 103(a)

Claims 22-26 and 28-29 are rejected as being obvious over Lang (US 5,675,654). Lang discloses a multi-channel network device for interfacing between a plurality of physical data links and a control processor, where each physical data link transmits a data stream of data packets communicated according to a data link control protocol, preferably High-Level Data Link Control (HDLC). In contrast, the present invention is directed to devices and methods for processing data that are multiplexed onto a single transport stream broadcast to multiple receivers and communicated according to a Moving Pictures Experts Group (MPEG) protocol (see the specification, page 1, line 17-22; page 11-13). Lang distinguishes his device, which is capable of handling a variety of data streams, each having different interface rates and having a multiplicity of possible channelized and unchannelized configurations, from previous devices that encode or decode a single data stream (see, for example, col. 1, lines 1-49).

Lang teaches that the network device includes a plurality of line interfaces, each of which is operative to receive incoming data segments and has at least one channel associated therewith. A channel assigner circuit assigns each incoming data segment to one of its channels and pipelines the incoming data segments downstream to a time-slice data processor. Ones of the pipelined incoming data segments are processed by the data processor according to information in associated state vectors. Each pipelined incoming data segment is stored in one of a plurality of FIFO buffers, each corresponding to one of the data channels. Lang further teaches that a plurality of data packet descriptors is maintained in a packet management circuit, each descriptor referencing a first memory block capable of holding one of the pipelined incoming data segments. The packet management circuit transfers the data segments stored in the channel FIFO buffers to the first memory blocks via a control processor interface and manages the transfer with the data packet descriptors. See, for example, col. 6, line 48 - col. 7, line 35.

Therefore, contrary to the examiner's contention, Lang does not teach associating each DMA channel with a specific location in the host computer memory by storing a context in local memory for each DMA channel, which context includes a pointer to frame descriptors including

specific host memory block information. Rather, Lang teaches storage of data segments in channel-specific FIFO buffers in HDLC processor (22), and the transfer of data from each FIFO buffer to host memory by a DMA controller (24) through a PCI controller (26) into host computer memory (e.g. see Figs. 3 and 4). The DMA controller (24) is not directly connected to the host memory PCI bus (as shown in Fig. 1 of the present application), and memory accesses are serviced by a downstream PCI controller (26) using packet descriptors that contain the size and location of data buffers in host memory and the data packet information associated with the data in each buffer. See, for example, col. 17, lines 45-59.

First of all, one skilled in the art would not be motivated to combine the teachings of Ryan and Lang because Lang relates to the managing of multiple data streams communicated according to HDLC protocol, whereas Ryan relates to the parsing of a single transport stream communicated according to an MPEG protocol into multiple elementary streams. Secondly, even if there was a motivation to combine references, the combination does not teach the claimed invention because Lang does not clearly teach the limitation of storing a context in local memory for each DMA channel, which context contains a pointer to a frame descriptor in local memory, each of which contains the specified information regarding the host memory. For these reasons, it is respectfully submitted that amended claims 22-26 and 28-29 avoid the rejection of record.

With regard to claims 24-26, the Examiner cites Lang as curing the deficiency of Ryan to clearly disclose the step of transferring the multiple elementary streams to an end user system comprises transferring the multiple elementary streams through an audio-visual/network interface. Contrary to the Examiner's contention, nowhere does Lang teach or suggest that the multi-channel network device transfers multiple elementary streams through an audio-visual or a networked computer interface as described in the present invention. As set forth in the Summary of the Invention, Lang discloses a multichannel network device for interfacing between a plurality of physical data links and a single control processor, where each physical data link is characterized by a data stream of data packets communicated by a data link control protocol. See col. 1, lines 52-57. Hence, Lang relates to a digital communications network having a high density encoder and decoder capable of handling a variety of data streams, not multiple elementary streams parsed from a single transport stream as described in

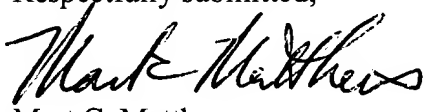
the present invention. See col. 1, lines 14-16. The multiple data streams described in Lang, e.g. those communicated according to HDLC protocol, are presented according to telephonic convention (see, e.g. col. 29, lines 48-53), and there is no teaching or suggestion that multiple elementary streams, e.g., MPEG elementary streams, are transferred to an audio-visual system through an audio-visual interface, or to a networked computer system through a network interface. As shown in Fig. 3, the device of Lang (element 10) couples only to a single host computer located on uplink side 14, which receives and transmits data through the device 10, not to an end user system such as a networked computer system or audio/visual system. For these reasons, there is no suggestion in the references themselves to combine the teachings of Ryan and Lang, and even if combined, the combination of Lang with Ryan does not lead one to the invention of claims 24-26. Withdrawal of the rejection and allowance of the claims is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,



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